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A close proximity self-aligned shadow mask for sputter deposition onto a membrane or cavity

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Abstract
In this paper we report on the fabrication of a close proximity shadow mask designed for sputtering into cavities or onto the back surface of freestanding silicon nitride (SiN_x) membranes. Sputtering into a well-defined area on a fragile surface is difficult since sputter deposition through a shadow mask separated from the deposition surface typically results in spreading of the deposited material. The area of spreading beyond the desired area of deposition depends on the vertical separation between the shadow mask and the surface of the membrane. In our design, a high degree of accuracy (± 5 μm) in the separation (25 μm) between the shadow mask and the deposition surface is achieved. The shadow mask is made from SiN_x-coated silicon wafers, using potassium hydroxide (KOH) etching on both sides of the wafer. The design rules chosen to maintain accuracy of the fit between the shadow mask and the deposition surface over various etch conditions, fabrication and methods used for convex-corner compensation and the alignment to the wafer crystal axis, which also contribute to an accurate fit, are discussed. Spreading of deposited material due to sputtering is limited to about 40 μm when this shadow mask is used.

1. Introduction

MEMS chip calorimeters have been used since the mid 1990s [1–4] in many material studies. These include size-dependent properties of nanoparticles [5, 6], specific heat measurements of magnetic materials [7], polymers [8, 9]. The nano-differential scanning calorimetry (nanoDSC) device developed in our lab uses a SiN_x membrane [10–12]. In these devices, the sensor heater strip is typically patterned on the top surface of the membrane, while the material to be tested is deposited or sputtered onto the back surface of the membrane [2, 12]. The thin membrane allows heating of the test material by application of currents below 100 mA to the heater strip. The material is deposited onto a given area of the membrane by the use of a shadow mask. In this paper we describe a method for fabricating a self-aligning shadow mask for accurately depositing thin films on to the membrane. Similar calorimetric techniques including shadow mask were mentioned by other groups [2, 4] and initially brought to our attention by Hellman's group [2], however neither the design of the shadow mask, nor the accuracy of the fit have been discussed in these cases. Brugger *et al* [13] discuss a similar shadow mask design for patterning onto a deeply recessed surface. In their design, the shadow mask is etched at the opening from both top and bottom surfaces. Since a convex corner would form at the critical dimension (width of shadow mask opening) in this method, the width and also the distance between the deposition surface and the shadow mask critical dimension would strongly depend on the etch parameters and control over the endpoint of the etch. In our design, we emphasize the accuracy of the fit and repeatability of feature sizes. The accuracy of the dimensions is improved by etching the opening from only one side, taking into account the alignment to crystal axis, and also taking into account the influence of different etch conditions—

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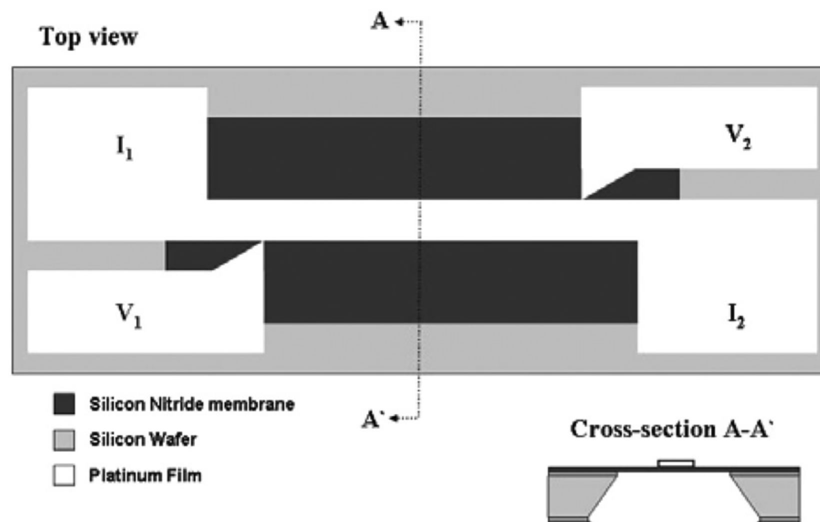

Figure 1. Schematic diagram of a nanoDSC sensor.

which result in variable etch selectivity of the (1 0 0):(1 1 1) planes, and hence could cause different undercuts. Error in the fit between the sensor and shadow mask has been limited to $\pm 5\ \mu$m.

Figure 1 shows a schematic diagram of the nanoDSC sensor. It consists of a freestanding rectangular silicon nitride (SiN_x) membrane fabricated by etching through a 100 nm SiN_x coated (1 0 0) silicon wafer using the KOH etch. Since the KOH etch is highly anisotropic with respect to the (1 0 0) and (1 1 1) planes, the cavity below the membrane has walls at an angle of 54.74° to the surface. A platinum (Pt) strip of 50 nm thickness and 500 μm width, connected to four contact pads, is deposited onto the membrane by electron beam evaporation and lift-off, after photolithography. This strip of Pt is the active area or the calorimetric cell of the sensor and is used as the heater as well as the temperature sensor of the calorimeter. The resistance versus temperature characteristic of the sensor is pre-calibrated. The test material is deposited on the back surface of the membrane in the area opposite to the Pt strip. Current is passed through the current leads I_1 and I_2 to heat the Pt strip, and the voltage across terminals V_1 and V_2 is measured to obtain the resistance, and hence the temperature of the cell. From the power delivered to the cell, and the resulting temperature, heat capacity and enthalpies are calculated [10, 12].

In the operation of our adiabatic nanocalorimetry sensor, it is critical to deposit the sample film on the insulating side of the membrane (back surface) with accurate lateral alignment so that the sample is directly below the heater strip. Otherwise, obtaining a quantitative heat capacity value (Cp) via the typical analysis methods [10] used for this device becomes difficult. For example, if the sample is wider than the heater (overshoot condition) the extended portion of the sample will shunt heat to the membrane and introduce uncertainty in the amount of material which is actually being sampled. Correction for this overshoot could be accomplished perhaps with finite-element analysis but it is prohibitively time consuming, especially if there are sample-to-sample variations in the amount and spatial regularity of the overshoot. Likewise if the sample width is narrower than the heater then the temperature uniformity of the heater could be compromised. Even more troublesome is the case where the shadow mask is rotated to some extent so that both overshoot and undershoot occur simultaneously. Therefore, a good alignment of the deposited material with the heater strip is essential.

If sputtering is the deposition method of choice, high partial pressure of the sputtering gas during deposition and the resulting low mean free path of particles causes the deposited material to spread around corners of the shadow mask. Therefore, the shadow mask must be as close as possible to the membrane in order to restrict deposition to the desired region. The shadow mask is designed to fit the exact measured final width of the sensor cavity (1965 μm).

2. Experiment

We start with the requirement that the separation between the shadow mask and the sensor be 25 μm $\pm$ 5 μm when the sensor is placed directly on the mask. The sensor must be self-aligned on the shadow mask. A convenient way to do this is to use the KOH etch for the shadow mask in the same way as the sensor so that the angles are naturally similar [13]. Allowing the sensor to rest on the walls rather than on the base of the shadow mask gives a better accuracy since the depth of the etch is hard to control to within a few microns. The KOH etch results in a wide angle (54.74°) at the opening, providing the sputtered material with a wider access to the membrane, and allowing a uniform film to be deposited.

The design of the shadow mask is shown in figure 2. The fabrication sequence is shown in figure 3. Boron-doped $\langle 1\,0\,0\rangle \pm 0.9°$, 100 mm diameter, 700 μm nominal thickness, double side polished wafers are used for the experiment. A 100 nm thick low stress SiN_x film is deposited directly on the wafers by low-pressure chemical vapor deposition (LPCVD). The shadow mask fabrication requires three KOH etch steps. The first step involves finding the [1 1 0] axis of the wafer.

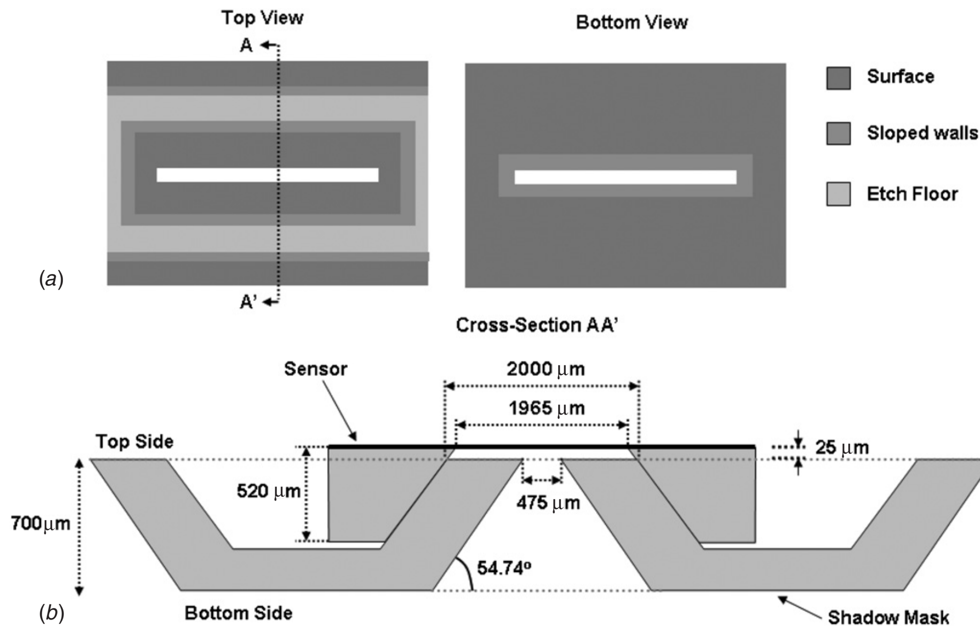

Figure 2. Design of the shadow mask. (*a*) Top and bottom views. (*b*) Cross-sectional view of the sensor resting on the shadow mask. Desired critical dimensions of the shadow mask are shown.

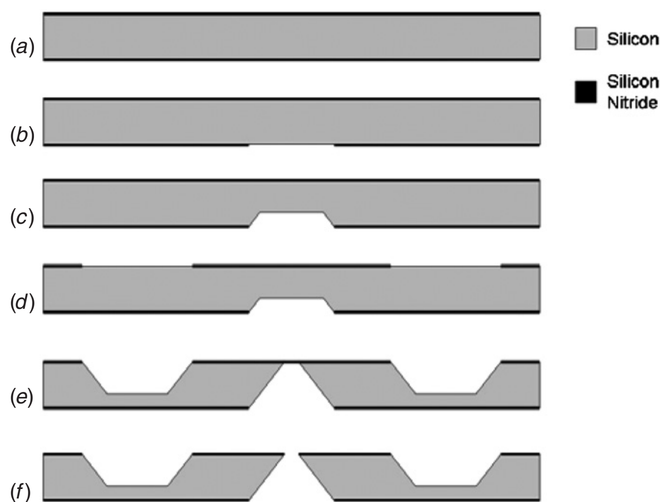

Figure 3. Schematic diagram of the sequence of steps for the fabrication of the shadow mask.

Alignment marks showing the crystal axis are formed in an initial 15 min etch step. Subsequent stages are aligned to these marks using an Electronic Visions EV620 contact aligner with back-side alignment. The bottom side is first aligned to the crystal axis and patterned using photolithography. The top side and the wafer edge are coated with photoresist to protect the SiN_x in these areas. Descum of exposed areas is done using oxygen plasma for 10–20 s. The SiN_x layer is then etched in the exposed areas using plasma etching in 5.33 Pa (0.04 $\times$ 10^{-3} Torr) of CF_4 gas for 5 min (figure 3(*b*)). The photoresist is then stripped and silicon etching is started. Silicon etching is done in a 25% aqueous KOH solution at a temperature of 90 $\pm$ 5 °C. The wafers are etched on both sides to different depths by using the staggered etching procedure shown in figures 3(*a*)–(*f*). The etch depth on the top side must be greater than 495 μm, while the bottom side has to be etched through the wafer (700 μm). This is done by pre-etching to a depth larger than 205 μm (=700 μm–495 μm) on the bottom side of the wafer (figure 3(*c*)) before the top-side patterning is done. The wafers are then taken out of the KOH solution, cleaned, coated with a photoresist, and patterned on the top side using back-side alignment. After removing the top SiN_x layer (figure 3(*d*)), silicon on the bottom side is etched completely (figure 3(*e*)). To preserve the correct dimensions of the shadow mask opening, overetching should be avoided. Finally, the free-standing membrane is removed before using either manually or using ultrasound (figure 3(*f*)).

2.1. Crystal axis alignment

The alignment of the shadow mask as well as the sensor features to the crystal axis of the wafer is crucial for repeatable performance of shadow masks from different wafers. Since KOH etching proceeds along the crystal axis, a small misalignment of the pattern with respect to the crystal ⟨1 1 0⟩ direction during the first etch (SiN_x etch) would result in larger than expected dimensions for cavities (figure 4(*a*)) and smaller than expected dimensions for plateaus or mesas. For small features with sufficient etch time, a cavity would reach the (1 1 1) crystal planes and take the shape shown in figure 4(*a*). For long rectangular features in the currently used devices, errors in width of tens of microns could occur. For an 8 mm $\times$ 2 mm feature (figure 4) a 1° error in the alignment would result in an error in width of a maximum of 8 mm $\times$ tan(1°) i.e., 140 μm, though, in practice the error is generally much smaller. However, since the maximum error desired in the vertical direction for this design is only $\pm$5 μm, the corresponding maximum error in the horizontal direction is $\pm$7 μm. This accuracy can be guaranteed only by pre-aligning the features to the crystal axis. Alignment to the crystal axis must be done for all shadow masks as well as sensor wafers to achieve a good fit.

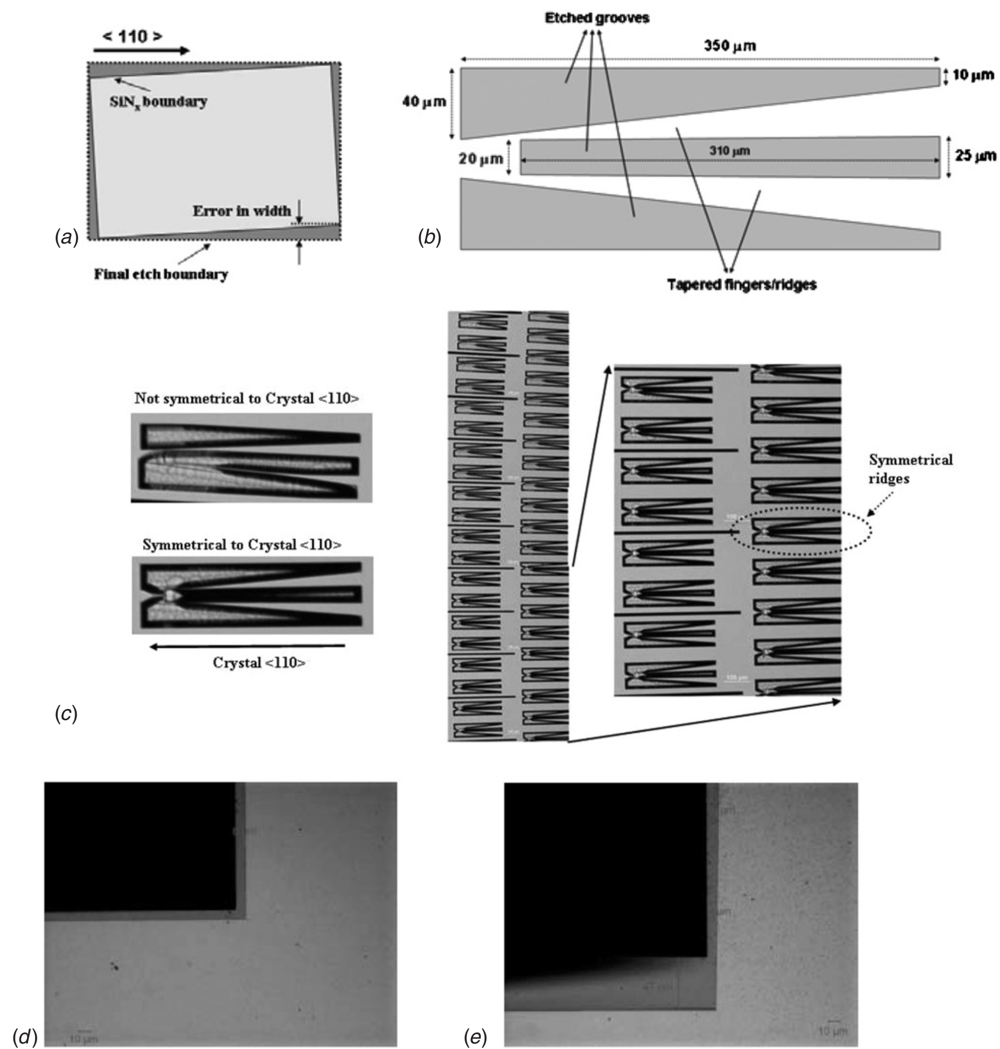

Figure 4. Alignment to the crystal axis of the wafer. (*a*) Change in width of a small cavity due to misalignment, after a long KOH etch. (*b*) Design of the asymmetrical etch features (alignment fork) used to determine the degree of misalignment from the crystal axis. (*c*) Image of the array of etch features. (*d*), (*e*) Comparison between a wafer with crystal axis alignment performed (*d*) and the one without (*e*). The badly misaligned wafer (*e*) results in an etch pit with wider dimensions.

Many schemes to find the crystal axis by etching have been proposed. We considered two possibilities: one is a curved array of asymmetric angular features [14], and the other a curved array of circular features [15]. The first method is more useful for our application since the features are very clearly visible even through a coating of photoresist.

The design of the alignment pattern called 'fork' with angular features is shown in figure 4(*b*). After a 15 to 20 min etch in a 25% aqueous KOH solution at 90 ± 5 °C, the geometry results in two tapering fingers/ridges. If the alignment fork is perfectly parallel to the crystal ⟨1 1 0⟩ direction, the etch would happen symmetrically. However, if the fork is misaligned from the ⟨1 1 0⟩ direction, asymmetrical etching results in ridges of different lengths (figure 4(*c*)). We arrange these crystal alignment forks as an array in ± 3° arcs on the two opposite ends of the wafer. The step size of the array sets the accuracy that can be achieved through this alignment process to 0.125°. Figure 4(*c*) shows the array on one side of the wafer. The asymmetry between the two triangular fingers/ridges in each progressively decreases as we move down. The only fork which has symmetrical ridges (circled with the dotted line in figure 4(*c*)) is selected on each side. A line joining these two forks would be parallel to the crystal ⟨1 1 0⟩ direction. Subsequent photomasks are aligned to these two forks.

Figure 4(*d*) shows a corner of an etch pit in a wafer where crystal alignment was done. The overhanging SiN_x membrane is caused due to slow etching of the (1 1 1) planes and is 8 μm in both directions. For comparison, figure 4(*e*) shows an etch pit on a wafer with a strong misalignment between the features and the ⟨1 1 0⟩ direction. The undercut is asymmetric, and the feature is 39 μm over-etched along the width dimension.

2.2. *Design of the shadow mask*

Figure 5 shows the dimensions of the features used in the photolithographic masks for the top and bottom surfaces. The design is based on an opening of width 475 μm. The thickness of the wafer is assumed to be 700 μm. Therefore, for an opening of 475 μm, the width of the initial bottom side etch

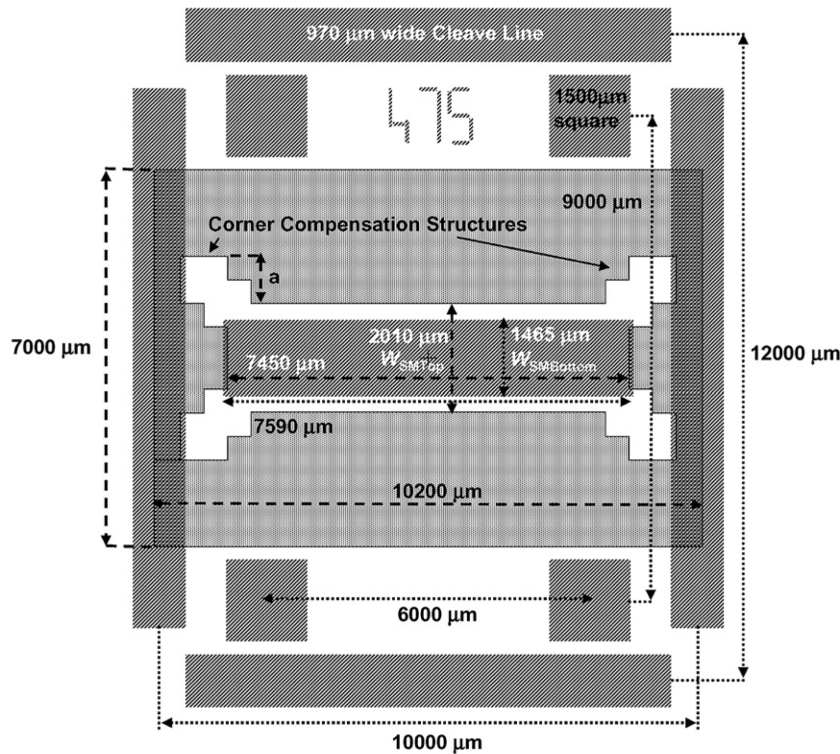

Figure 5. Layout of the photolithographic masks for the top and bottom sides of the shadow mask. The striped areas represent the bottom side photomask, and the gray area enclosed in a boundary line represents the top side photomask.

feature would have to be 2∗700∗cot(54.74°) + 475, which is 1465 μm (figure 5). The other critical dimension is the post-etch total width of the top surface of the shadow mask mesa, which is required to be 2000 μm (figure 2). However, this critical dimension experiences an undercut during etching of the top surface (figures 3(*d*)–(*e*)). Experimentally, for our typical etchant (aqueous KOH solution) with a concentration of 25% and temperature of 90 ± 5 °C, the undercut for an etch depth of 520 μm is typically 8 μm on each side, giving a selectivity between the (1 0 0) and (1 1 1) planes to be 65:1. This is much smaller than typical quoted values of 400:1 [16], presumably due to the aggressive etch parameters used. To compensate for this undercut over a wide range of conditions, the width of the mesa is increased by 5 μm on each side in the design, making the total width 2010 μm (figure 5). This brings the expected separation between the shadow mask and the sensor to within the 25 ± 5 μm range for etch parameters resulting in an undercut anywhere between 1.5 μm and 8.5 μm. Additional features in the design include cleave lines, four positioning holes to provide automatic alignment of the shadow mask inside a sample holder and corner compensation structures for the top surface.

The key design rules used for the photolithographic masks are summarized below:

$$a = 1.838\,[t_{\mathrm{SWafer}} - D] - w_{\mathrm{Overetch}} \qquad (1)$$

$$W_{\mathrm{SMTop}} = W_{\mathrm{Sensor}} + 2D * \cot(54.74) + 2 * w_{\mathrm{Undercut}} \qquad (2)$$

$$W_{\mathrm{SMBottom}} = W_{\mathrm{Opening}} + 2t_{\mathrm{SMWafer}} * \mathrm{Cot}\,(54.74) \qquad (3)$$

$$d_{\mathrm{TopEtch}} > t_{\mathrm{SWafer}} - D, \qquad (4)$$

where a is the width of the corner compensation structure, t_{SWafer} is the sensor wafer thickness, t_{SMWafer} is the shadow mask wafer thickness, D is the desired separation between sensor and shadow mask, w_{Overetch} is the over-etch dimension of corner compensation structures for safety (∼35 μm used), W_{SMTop} is the width or length dimension of the top of the shadow mask mesa, W_{Sensor} is the measured width or length dimension of the cavity in the sensor, w_{Undercut} is the average undercut expected for etch depth d_{TopEtch} over the range of etch parameters to be used (5 μm), W_{SMBottom} is the width or length dimension for the etch feature on the bottom side of the shadow mask, W_{Opening} is the width or length dimension of the desired shadow mask opening, d_{TopEtch} is the etch depth on the top side of the wafer.

2.3. Corner compensation

Since the shadow mask should fit into the cavity of the sensor, it has the convex shape of a rectangular mesa. However for such a shape, higher order crystal planes would be exposed at the corners. These planes are etched much faster than the (1 0 0) or (1 1 1) planes [16, 17]. A number of methods have been proposed to tackle the convex-corner etching [16–20]. The key feature among all these methods is the addition of structures at the convex corners which in effect move the susceptible corner further away from the device area (point P to point Q in figure 6(*a*)). By choosing the dimensions of these features appropriately in relation to the desired etch depth, the corner can be preserved until the etch in the vertical direction is completed. We use the method presented by Fan and Zhang [16], due to the small footprint required by these

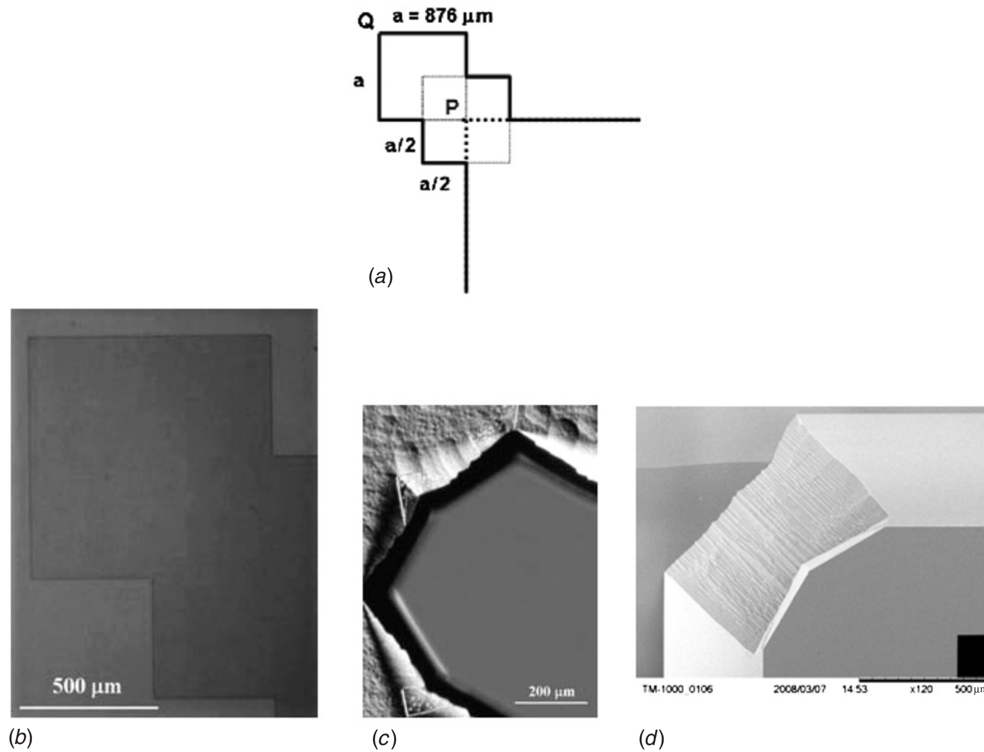

Figure 6. Corner compensation structure at different stages of etching. (*a*) Schematic diagram. (*b*) Before KOH etch, and after SiN_x was patterned. (*c*) After 2 h of KOH etch. (*d*) After completion of the etch (5 h).

compensation structures. This method uses two overlapping squares added at each corner (figure 6(*a*)). The dimensions of these structures are determined by the equation [16]

$$a = \frac{H}{\left[\frac{0.472}{U_C} + 0.221\right]}, \quad (5)$$

where a is the side of the square, H is the etch depth and U_C is the etching rate ratio (Etch rate of $\langle 410\rangle$/Etch rate of $\langle 1\,0\,0\rangle$). This is valid assuming the condition $U_C < 1.75$ is satisfied.

The requirement of this application is to have convex corners that are perfectly etched or mildly over-etched, but not under-etched. Given this freedom, the following two approximations are used: (1) use the value of U_C quoted for a 30% KOH etch solution kept at 80 °C ($U_C = 1.46$) [16]; (2) assume that $U_C < 1.75$ for our etch parameters. Under these conditions, and for a minimum etch depth of 495 μm, the value of a should be ~910 μm. The value of a is chosen to be 876 μm to allow mild over-etching at the convex corner for safety. Experimentally we find that these are reasonable approximations. Figure 6 shows the corner compensation structure before (figure 6(*b*)), during (figure 6(*c*)) and after (figure 6(*d*)) the KOH etch. The corners are over-etched as expected, but the rest of the mesa has been protected.

3. Results

The top and bottom surfaces of the completed shadow mask are shown in figures 7(*a*) and (*b*). Figures 7(*c*) and (*d*) show scanning electron microscope (SEM) images of the top and bottom surfaces of the shadow mask. In order to see the alignment of the sensor on the shadow mask, we remove the membrane on a sensor, and place it on the shadow mask as shown in figure 7(*e*). The sensor is self-aligned symmetrically on the shadow mask. Figure 7(*f*) shows a complete sensor placed on the shadow mask. The shadow mask can be seen faintly through the SiN_x membrane of the sensor. The opening of the shadow mask is well aligned to the Pt strip of the sensor. To see the alignment of the shadow mask opening to the Pt strip, we overturn the sensor and place the shadow mask on it (figures 7(*g*) and (*h*)). The Pt strip can be seen through the membrane and the shadow mask opening. Only the area under the platinum strip is exposed for test film deposition. Figure 7(*i*) shows the result of sputtering of silicon and nickel onto the sensor using the shadow mask. The deposited material is found to be well aligned in the horizontal direction with a misalignment of less than 10 μm. NanoDSC measurements of this and other films deposited using the shadow mask will be presented elsewhere.

The width of the opening in the shadow mask is designed to be 475 μm for a wafer thickness of 700 μm. The wafer thickness tends to vary between wafers and batches. If the same photomask is used for wafers of different thicknesses, the opening of the shadow mask would also differ. The other dimensions are not affected by the thickness of the wafer. For example, a wafer of thickness 705 μm would have an opening of $1495 - 2 * 705 * \cot(54.74°) = 468$ μm (equation (3)). The measured dimensions of a shadow mask fabricated, are shown in Figure 7(*k*). The horizontal dimensions are measured using an optical microscope with a RSF Elektronik MSA 001 linear encoder and Boeckler 2-MR digital readout, which has a 1 μm resolution and a calibration accuracy of about 0.04%.

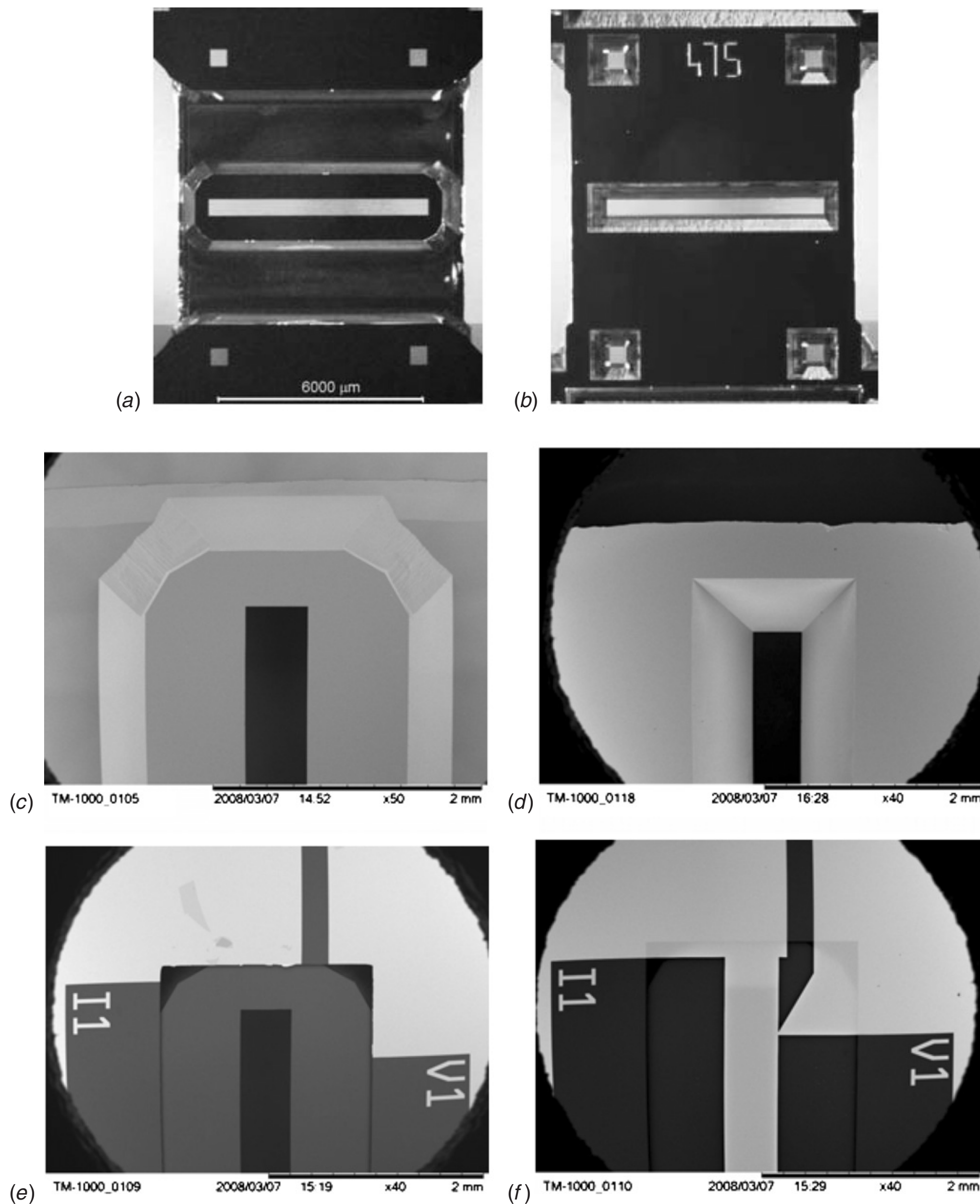

Figure 7. (*a*), (*c*) Top and (*b*), (*d*) bottom surfaces of the final shadow mask, respectively. (*e*) Sensor with membrane removed, self-aligned on a shadow mask. (*f*) Sensor with membrane self-aligned on the shadow mask. The shadow mask can be seen faintly through the SiN_x membrane. (*g*), (*h*) Shadow mask placed on an overturned sensor and self-aligned to the sensor. The bright area is the Pt film of the sensor seen through the sensor's SiN_x membrane. Alignment is good both on the top and bottom ends. (*i*) Image of a back side of the sensor with a thin film deposited using the shadow mask. The dark regions are areas with a bare SiN_x membrane. The areas of medium brightness are the areas where Pt is on the other side of the SiN_x membrane. The brightest area in the center is the deposited test film. (*j*) Cross section of a film deposited through the shadow mask. (*k*) Dimensions of final shadow mask.

The measured values of the top width of the mesa, and the width of the shadow mask opening, have been found to be uniform to within ± 1 μm across a single 4 inch wafer, and also from one wafer to another in the same batch.

From figure 7(*j*) the total width of the deposited film is measured to be about 560 μm. The spread of the sputtered material is (560–468)/2 i.e., about 45 μm in each direction beyond the opening in the shadow mask, at an argon sputtering pressure of 0.587 Pa (4.4 $\times$ 10^{-3} Torr). Using a profilometer and by placing a sensor with a removed membrane on top of a shadow mask (figure 7(*e*)), the actual separation between the sensor and the top of the shadow mask is measured to be about 28 μm, which is very close to the design value of 25 μm. Since the sensor rests on the side walls of the shadow mask, misalignment in the *x*–*y* direction is minimal when the sensor is placed horizontally on the shadow mask. However, there is a possibility of a tilt in the placement of the sensor on the shadow mask which could cause asymmetric deposition. The degree of tilt is limited by the distance between the bottom surface of the sensor and the bottom surface of the etched area on the top side of the shadow mask. By controlling the pre-etch depth of the shadow mask bottom surface (figure 3(*c*)) to be close to 205 μm, this distance could be minimized, and the tilt can be restricted. The shadow mask

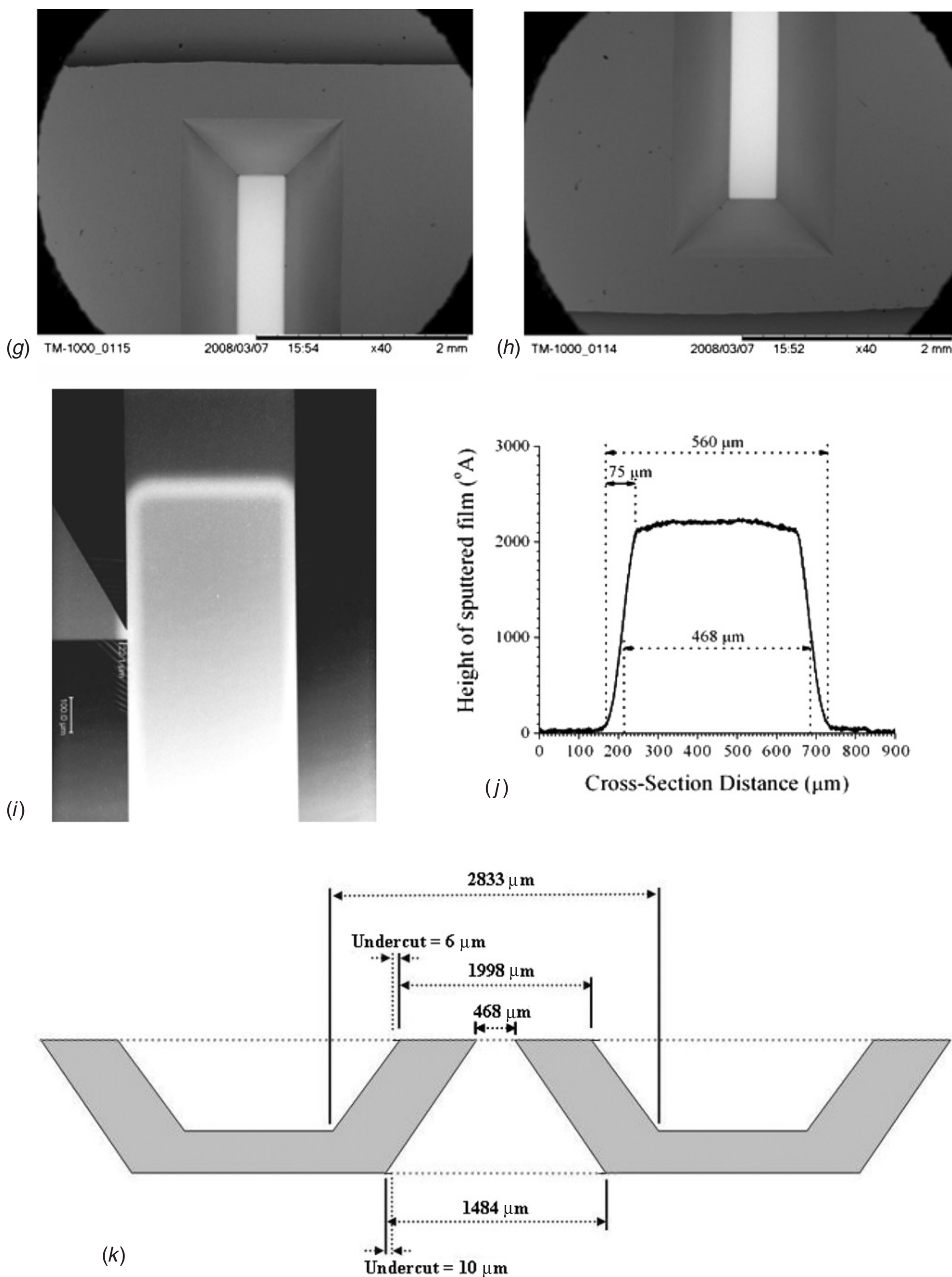

Figure 7. (Continued.)

can be reused indefinitely, provided the deposited films do not alter the width of the opening due to accumulation.

4. Conclusion

The need for sputtering onto a well-defined area on the nano-DSC membrane has motivated the fabrication of this close proximity self-aligned shadow mask. With this device, precisely aligned sputtering onto the back surface of the sensor's membrane has been achieved. The vertical separation between the mask and the sensor is designed to be 25 ± 5 μm. The actual separation measured after mask fabrication is 28 μm and stays within the designed range. Spreading of sputtered material is about 45 μm in each direction. The general design principles implemented here can be used for close proximity shadow masking for precise sputtering onto other membrane or cavity-based devices.

Acknowledgments

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References

[1] Cavicchi R, Semancik S, Suehle J S and Gaitan M 1994 Application of microsubstrates for materials processing *USA Patent* 5356756

[2] Denlinger D W, Abarra E N, Allen K, Rooney P W, Messer M T, Watson S K and Hellman F 1994 Thin film microcalorimeter for heat capacity measurements from 1.5 to 800 K *Rev. Sci. Instrum.* **65** 946–59

[3] Sarro P M, van Herwaarden A W and van der Vlist W 1994 A silicon-silicon nitride membrane fabrication process for smart thermal sensors *Sensors Actuators* A **42** 666–71

[4] Suh K S, Kim H J, Park Y D, Kim K H and Cheong S-W 2006 Development and characterization of a microcalorimeter based on a Si-N membrane for measuring a small specific heat with submicro-Joule precision *J. Korean Phys. Soc.* **49** 1370–8

[5] Efremov M Y, Schiettekatte F, Zhang M, Olson E A, Kwan A T, Berry R S and Allen L H 2000 Discrete periodic melting point observations for nanostructure ensembles *Phys. Rev. Lett.* **85** 3560

[6] Lai S L, Guo J Y, Petrova V, Ramanath G and Allen L H 1996 Size-dependent melting properties of small tin particles: nanocalorimetric measurements *Phys. Rev. Lett.* **77** 99

[7] Abarra E N, Takano K, Hellman F and Berkowitz A E 1994 Heat capacity measurements of antiferromagnetic CoO/NiCoO superlattices *J. Appl. Phys.* **76** 6292

[8] Adamovsky S A, Minakov A A and Schick C 2003 Scanning microcalorimetry at high cooling rate *Thermochim. Acta* **403** 55–63

[9] Efremov M Y, Olson E A, Zhang M, Zhang Z and Allen L H 2003 Glass transition in ultrathin polymer films: calorimetric study *Phys. Rev. Lett.* **91** 085703

[10] Efremov M Y, Olson E A, Zhang M, Lai S L, Schiettekatte F, Zhang Z S and Allen L H 2004 Thin-film differential scanning nanocalorimetry: heat capacity analysis *Thermochim. Acta* **412** 13–23

[11] Efremov M Y, Olson E A, Zhang M, Schiettekatte F, Zhang Z and Allen L H 2004 Ultrasensitive, fast, thin-film differential scanning calorimeter *Rev. Sci. Instrum.* **75** 179–91

[12] Olson E A, Efremov M Y, Ming Z, Zishu Zhang and Allen L H 2003 The design and operation of a MEMS differential scanning nanocalorimeter for high-speed heat capacity measurements of ultrathin films *J. Microelectromech. Syst.* **12** 355–64

[13] Brugger J, Andreoli C, Despont M, Dreschsler U, Rothuizen H and Vettiger P 1999 Self-aligned 3D shadow mask technique for patterning deeply recessed surfaces of micro-electro-mechanical systems devices *Sensors Actuators* A **76** 329–34

[14] Vangbo M and Backlund Y 1996 Precise mask alignment to the crystallographic orientation of silicon wafers using wet anisotropic etching *J. Micromech. Microeng.* **6** 279–84

[15] Ensell G 1996 Alignment of mask patterns to crystal orientation *Sensors Actuators* A **53** 345–8

[16] Fan W and Zhang D 2006 A simple approach to convex corner compensation in anisotropic KOH etching on a (1 0 0) silicon wafer *J. Micromech. Microeng.* **16** 1951–7

[17] Wacogne B, Zeggari R, Sadani Z and Gharbi T 2006 A very simple compensation technique for bent V-grooves in KOH etched (1 0 0) silicon when thin structures or deep etching are required *Sensors Actuators* A **126** 264–9

[18] Enoksson P 1997 New structure for corner compensation in anisotropic KOH etching *J. Micromech. Microeng.* **7** 141–4

[19] Pal P and Chandra S 2004 A novel process for perfect convex corner realization in bulk micromachining *J. Micromech. Microeng.* **14** 1416–20

[20] Zhang Q, Liu L and Li Z 1996 A new approach to convex corner compensation for anisotropic etching of (1 0 0) Si in KOH *Sensors Actuators* A **56** 251–4