Au-mediated low-temperature solid phase epitaxial growth of a Si_xGe_{1-x} alloy on Si(001)

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The evolution of microstructure during Au-mediated solid phase epitaxial growth of a Si_xGe_{1-x} alloy film on Si(001) was investigated by *in situ* sheet resistance measurements, x-ray diffraction, conventional and high-resolution transmission electron microscopy, energy dispersive x-ray spectroscopy, and Rutherford backscattering spectrometry. Annealing amorphous-Ge/Au bilayers on Si(001) to temperatures below 120 °C caused changes primarily in the microstructure of the Au film. Near ≈130 °C, Ge from the top layer diffused and crystallized along the grain boundaries of Au. The Ge that had reached the Au/Si (001) interface mixed with Si from the substrate, to form epitaxial Si_xGe_{1-x} islands on Si (001). Si from the substrate had dissolved into Au before entering the growing epitaxial islands. Meanwhile, the Au that was displaced by Ge that filled the Au grain boundaries, diffused into the top layer along columnar voids in the amorphous Ge film. With increasing temperature, more Au was displaced to the top by the flux of Ge towards the substrate, facilitating further epitaxial growth and the coalescence of epitaxial Si_xGe_{1-x} islands. At 310 °C, the initial Au film was displaced completely to the top by a laterally continuous Si_xGe_{1-x} epilayer of uniform composition ($x \approx 0.15$). The epilayer thickness was limited by that of the initial Au film. Twins and residual amounts of Au trapped near the Si_xGe_{1-x}/Si(001) interface were the predominant defects observed in the completely strain-relaxed Si_xGe_{1-x} epilayer. © *1996 American Institute of Physics.* [S0021-8979(96)05405-7]

I. INTRODUCTION

SiGe alloys form the basis of exceptionally high speed heterojunction bipolar transistors that surpass the speed of devices based on conventional Si technology.[1–3] The performance of these devices is dependent on the fabrication of a high quality epilayer of a SiGe alloy on a Si substrate, with a composition tailored to obtain the required lattice mismatch (e.g., $Si_{0.7}Ge_{0.3}$ for ~1.2% strain).[4] While the growth of SiGe films by molecular beam epitaxy (MBE), chemical vapor deposition (CVD), and laser assisted deposition processes yield fairly good quality epilayers, the high temperatures involved in these techniques (>600 °C) produce undesirable effects.[5–7] For example, high temperatures result in dopant redistribution and generation of unacceptable levels of defects such as threading dislocations.[8] Owing to these factors, it is worthwhile to explore alternative low-temperature epitaxial growth techniques.

Metal-mediated solid phase epitaxy (SPE) has been studied in a variety of systems and the advantages of this type of SPE are well known.[9] In addition to low temperatures, the adaptability of SPE for selected area and conformal growth of epilayers, and growth of semiconductor on insulator structures are some of the attractive features of SPE.[10,11] In this type of SPE, growth of Si or Ge is accomplished at low temperatures by using a eutectic-forming metal (e.g., Au, Al, Ag, etc.) as a transport medium. SPE growth can also be achieved by using a compound transport medium which is usually a silicide or a germanide of a near noble metal (e.g., Pd, Pt), obtained by the reaction of the metal with the substrate.[9] In either case, the epitaxial growth is effected by a post-deposition thermal anneal of samples with the metal (or compound) transport medium sandwiched between a layer of amorphous semiconductor and a single crystal substrate. In the past, metal-mediated SPE has been used mainly for epitaxial growth of elemental Si or elemental Ge on various substrates.[9] Recently, metal-mediated SPE has been receiving attention as a potentially useful alternative to MBE and CVD for low-temperature growth of heteroepitaxial layers of alloys. Hong and co-workers,[12,13] were the first to demonstrate the growth of a heteroepitaxial SiGe alloy film on Si(111) using Pd-mediated SPE. They allowed the metal layer to react with the substrate to form Pd_2Si which acted as the transport medium. But, attempts to grow SiGe on a single crystal Si(001) substrate (sc-Si) by using Pd were unsuccessful due to the formation of polycrystalline Pd_2Si.

Recently it was demonstrated that Au-mediated SPE could be harnessed to grow heteroepitaxial Ge-rich SiGe alloys on Si(001) during annealing bilayers of *a*-Ge/Au on sc-Si at low temperatures (≈300 °C).[14] While this is a promising first step, the need for a fundamental understanding of various phenomena occurring during the SPE growth process cannot be overemphasized. Such an understanding is essentially for the control of parameters like the composition (and hence the lattice mismatch) of the SiGe epilayer, necessary to obtain the desired change in the band structure to fabricate high-speed devices based on SiGe/Si heterostructures.[1–4]

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Also, issues like control of defect formation during growth, and elimination of Au (a deep level dopant) from the epilayer need to be addressed closely. In order to do this, the sequence of processes leading to SPE growth, their temperature dependence, and mechanisms must be investigated.

On a more general note, there have been few studies that have attempted to address the details of the microstructural changes that occur in the different layers during metal-mediated SPE growth. In this article, we present results outlining the sequence of microstructural changes leading to the SPE growth of a Si_xGe_{1-x} alloy film on sc-Si during annealing of amorphous-Ge/Au/sc-Si thin film sandwiches. The results also shed light on the plausible microstructural changes that may be occurring in SPE growth processes that use other metal transport media such as Al, Ag, etc. It will be shown, for the first time, that Au-mediated epitaxial growth of Si_xGe_{1-x} on sc-Si begins at temperatures as low as 130 °C. With increasing temperature, the epilayer grows both laterally and vertically to yield a continuous Si_xGe_{1-x} epilayer of uniform composition on annealing to ≈300 °C.

II. EXPERIMENTAL DETAILS

The substrates used in this study were *B*-doped, high resistivity (3–5 Ω cm) sc-Si. High resistivity substrates were chosen to facilitate most of the current forced through the thin film sandwich to pass through the film(s) on the substrate, rather than through the substrate itself, during *in situ* sheet resistance measurements (see below). This ensured that the changes in resistance of the samples were sensitive to the microstructure of the thin films deposited on sc-Si. The substrates were degreased in trichloroethane, cleaned with acetone, isopropyl alcohol, and de-ionized (DI) water before being treated with 5% HF to remove the native oxide on the substrate. The sc-Si substrates were loaded in a thermal evaporator and pumped down to a base pressure of 4×10^{-7} Torr. Films of Au and Ge were sequentially deposited on sc-Si without breaking vacuum at rates of ≈1 and ≈2 nm/s, respectively; the pressure was 5×10^{-6} Torr during deposition. The thicknesses of Au and Ge layers were determined by means of a Dektak 3030 profilometer to be ≈170 and ≈500 nm, respectively. This was confirmed by cross-sectional transmission electron microscopy (TEM) and Rutherford backscattering spectrometry (RBS). Films of different thicknesses of Au, Ge/Au, and Ge were also deposited on thermally oxidized sc-Si wafers in order to characterize the role of the different isolated layers.

The thin film sandwiches of Ge/Au/sc-Si were annealed in a high-vacuum furnace, with a base pressure of 5×10^{-8} Torr, at a preset heating rate of 1 °C/min. The vacuum furnace apparatus is equipped with a spring-loaded four point probe in a Van der Pauw geometry, for monitoring the sheet resistance of the thin film sandwiches during annealing. The whole apparatus[11] is interfaced with a computer for temperature control and data acquisition. A few milliamperes (typically ~10 to 100 mA) of current was forced through two of the probes and the voltage drop was measured across the other two probes. The temperature of the thin film sandwich was measured by means of a thermocouple spot-welded to the sample-holder assembly, which was in good thermal contact with the sample. Thus, temperature and the sheet resistance of the thin film sandwiches were monitored *in situ* during the anneals to track microstructural changes. The temperatures reported in this article are estimated to be precise within ±5 °C.

The as-deposited and annealed films were examined by x-ray diffraction (XRD) in a Rigaku D-Max III diffractometer using monochromatic Cu K_α radiation. Rocking curves (ω scans) of the (004) XRD peak of the epilayer and θ–2θ scans were obtained to characterize the thin film sandwiches and the properties of the epilayer. The *d* spacings reported in this article are precise within ±0.0001 nm. Selected samples (after etching away the top layer when necessary) were bombarded with 2 MeV alpha particles in RBS experiments performed in the IBM geometry.[15] The alpha particles were incident on the sample at an angle of 7°. RUMP[16] was used to simulate backscattering profiles for various sample compositions and configurations. Simulated profiles were compared with the experimental data and the best fit was used to determine the epilayer composition.

Specimen cross sections were mechanically thinned, mounted on a cold stage (77 K) and milled to perforation by 5 keV Ar^+ ions for transmission electron microscopy, electron diffraction, and chemical microanalyses. A Philips CM-12 microscope operating at 120 kV was used for conventional and high-resolution TEM. A Vacuum Generators HB-501 scanning transmission electron microscope (STEM) operating at 100 kV, equipped with a 1 nm electron probe and an energy dispersive x-ray detector, was used for x-ray energy dispersive spectroscopy (XEDS) and microdiffraction.

III. RESULTS

Figure 1(a) shows the configuration of the as-deposited Ga/Au/sc-Si thin film sandwich. From electron diffraction [see Fig. 1(b)] and XRD analysis which showed no crystalline Ge peaks, it was inferred that the Ge film in the as-deposited sample was amorphous. XRD showed that the Au layer was polycrystalline with a (111) texture. The amorphous Ge (*a*-Ge) layer revealed a columnar void structure typical of thin *a*-Ge films deposited by thermal evaporation at low temperatures.[17,18] Further TEM analysis showed that the Au film was polycrystalline and the grain size was ≈60 nm. The sheet resistance of the as-deposited sandwich was measured to be 0.3 (±1%) Ω/□. The resistivity calculated from the sheet resistance, based on the thickness of the Au layer, was 5 (±15%) μΩ cm and was close to the resistivity of pure Au (2.3 μΩ cm).[19] Thus, most of the current forced through the sample passes through the Au layer rather than the *a*-Ge layer or the sc-Si substrate as the resistivities of Ge and Si are over six orders of magnitude greater than that of Au[19] for any appreciable current to pass through them at ambient temperatures.

Representative results of *in situ* resistance measurements are presented in Figs. 2(a) and 2(b). For temperatures below 70 °C, the sheet resistance changes during heating were reversible during cooling. At temperatures near 80–90 °C, the sheet resistance decreased irreversibly, and the decrease continued up to ≈120 °C. In this temperature range, the charac-

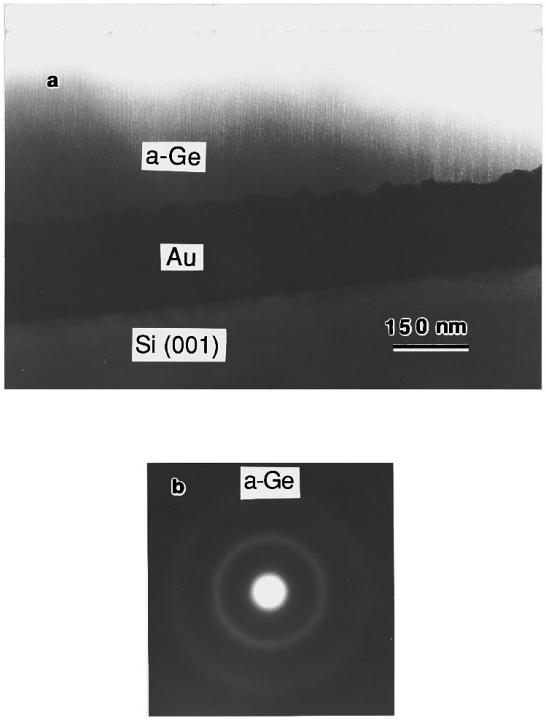


FIG. 1. (a) Bright-field TEM micrograph of the as-deposited thin film sandwich. The columnar void structure in the a-Ge film is clearly visible. (b) The diffuse rings in the diffraction pattern taken from the top layer shows that the as-deposited film of Ge was amorphous.

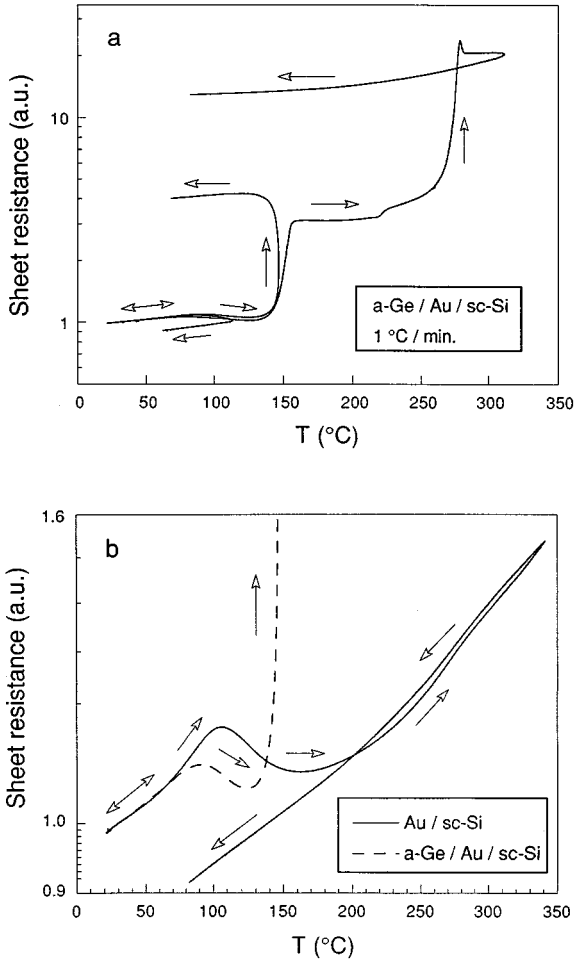
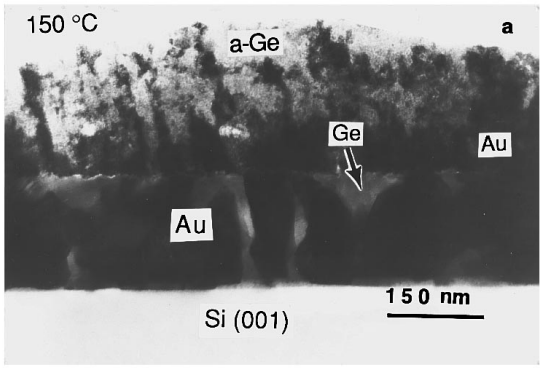


FIG. 2. (a) *In situ* sheet resistance (normalized to the initial value of 0.3 Ω/sq at 30 °C vs temperature behavior of a-Ge/Au/sc-Si during annealing. (b) A magnified version of the sheet resistance behavior of a-Ge/Au/sc-Si below 150 °C shown along with the resistance behavior of Au/Sc-Si (normalized to the initial value). Note the similarity in the resistance behavior of a-Ge/Au/sc-Si and Au/sc-Si below 150 °C. The resistance is plotted on a log scale in both figures.

teristics of the resistance-temperature behavior of Au/sc-Si [see Fig. 2(b)] and Au/SiO_2 were the same as that observed for a-Ge/Au/sc-Si. This indicated that the resistance changes between 90 and 120 °C were primarily due to changes occurring in the microstructure of the Au film. At ≈130 °C, the sheet resistance increased sharply and irreversibly to ≈2 to 5 times that of the unannealed sample. For $T>150$ °C, the resistance remained relatively insensitive to temperature up to ≈270 °C. Above ≈270 °C, the sheet resistance increased sharply to about 20–25 times that of the unannealed sample. The small blip in the resistance curve at ~225 °C was reproducible, but the reason for this change has not been investigated.

Annealing to 150 °C at 1 °C/min resulted in an increase in the height of the Au grains from ≈60 nm in the as-deposited case to ≈170 nm, i.e., the thickness of the Au film. Bright-field and dark-field TEM showed that Ge from the top amorphous layer diffused to the Au/sc-Si interface through the grain boundaries of the Au film as illustrated in Fig. 3(a). Microdiffraction of regions between the Au grains revealed that Ge (or possibly Si_xGe_{1-x}) had crystallized at the grain boundaries of the Au film. The columnar void structure had collapsed for the most part in the a-Ge layer. The top layer still consisted of amorphous Ge, except at localized regions where the Ge had crystallized as indicated by diffraction patterns in Figs. 3(b) and 3(c). Small crystallites (dark contrast in bright-field TEM) were observed to form at the initial a-Ge/Au interface. TEM and XEDS analyses showed that these crystallites consisted of clusters of Au and were embedded in locally crystallized Ge. In some regions, the crystallites formed streak-like patterns in the a-Ge film. The direction of the streaks was along the length of the columnar voids observed in the as-deposited film. This observation suggested that Au diffused along the columnar voids in the a-Ge film and interacted with the Ge, resulting in the streak-like patterns. The length of the streaks also indicated that Au had diffused to distances greater than 200 nm. In a-Ge/Au/sc-Si samples with a-Ge film thinner than 200 nm, visual inspection of the surface of the sandwiches annealed to 150 °C revealed a golden tinge confirming the rapid diffusion of Au to the top. Microdiffraction showed that Ge in the top layer had crystallized only in the regions where it had interacted with Au, while other regions in the top layer were still amorphous [see Fig. 3(c)]. Thus, only the Ge that had interacted with Au had crystallized.

Figure 4(a) depicts a closer view of the configuration of the initial Au layer after a 150 °C anneal. The thin continuous layer of dark contrast on top of the Au layer is a network of Au-rich crystallites. XEDS analysis illustrated in Fig. 4(b)



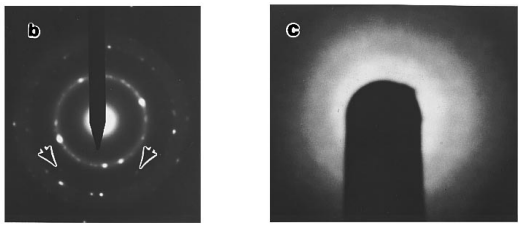
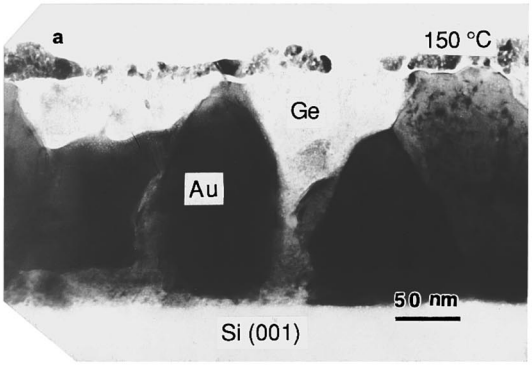


FIG. 3. (a) Bright-field TEM micrograph showing the microstructure of a sample annealed to 150 °C illustrates the incorporation of Ge between Au grains. Regions of dark contrast in the top layer are Au crystallites; note the streaks in the top layer. (b) The remnant amorphous halo in the diffraction pattern taken from the top layer illustrates that only part of the *a*-Ge film had crystallized. Au(111) reflections indicated by arrows show the presence of Au in the top layer. (c) A microdiffraction pattern taken in the Ge film, far away from the initial *a*-Ge/Au interface shows that the Ge that had not interacted with Au, had not crystallized.

qualitatively showed that the crystalline regions [regions of bright contrast in Fig. 4(a)] of Ge (or Si_xGe_{1-x}) between the Au grains in the Au layer had a significant amount ($\approx$15 at. %) of Si in it. So, the crystallized species between the Au grains was concluded to be a Si_xGe_{1-x} alloy with $x \approx 0.15$. From the XEDS analysis it was also noted that Au grains [see Fig. 4(b)] had a high concentration of Si in them. This concentration is much larger than the equilibrium solid solubility of Si in Au ($\approx$a few at. %) below 200 °C. Line scans along the height of the epitaxial islands [perpendicular to the line scan shown in Fig. 4(b)] showed that the Si concentration along the height of the crystallized islands was fairly uniform. Line scans across small Au particles dispersed in the epitaxial Si_xGe_{1-x} islands revealed a high concentration of Si.

XRD rocking curve scans on samples annealed to 130 °C showed that the (004) Si_xGe_{1-x} peak had a low linewidth (not corrected for instrumental broadening). This is illustrated by a representative rocking curve scan shown in Fig. 5. The position of (004) XRD peak indicated that the *d* spacing of the crystallized layer (0.1416 nm) was larger than that of pure Ge (0.1414 nm) implying that the Si_xGe_{1-x} alloy had compressive residual strain in the plane of the sc-Si substrate (see Sec. IV). These observations suggested that epitaxial growth of the Si_xGe_{1-x} on sc-Si had probably started in this temperature regime. Examination of the Au/sc-Si interface of samples annealed to 150 °C by high-resolution TEM confirmed that islands of the Si_xGe_{1-x} alloy had grown



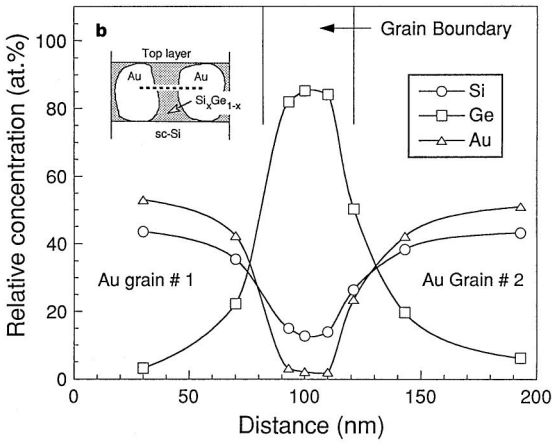


FIG. 4. (a) Bright-field TEM micrograph showing a closer view of the sample annealed to 150 °C depicting the Ge-rich Si_xGe_{1-x} regions (marked "Ge") between Au grains. Note the thin layer of Au-rich crystallites formed on the top of the initial Au film (at the initial Au–Ge interface). The top layer is completely milled away. (b) A representative XEDS line scan profile (dashed line in the schematic drawing) across Au grains in the middle layer of the sample illustrates the nominal Si composition of the Ge-rich Si_xGe_{1-x} regions between the Au grains to correspond to $x \approx 0.15$. Note the high concentration of Si in the Au grains.

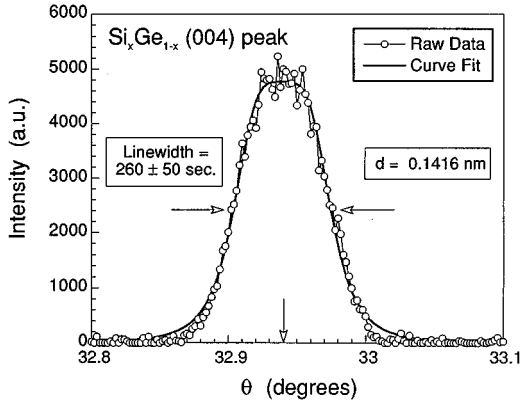


FIG. 5. XRD rocking curve of the Si_xGe_{1-x} (004) peak in a sample annealed to 130 °C. The Lorentzian fit (bold line) is superimposed on the raw data (open circles). In addition to the low linewidth, note the peak position that implies d_{SiGe} (measured) $> d_{\text{pure Ge}}$, measured perpendicular to the plane of the sc-Si substrate.

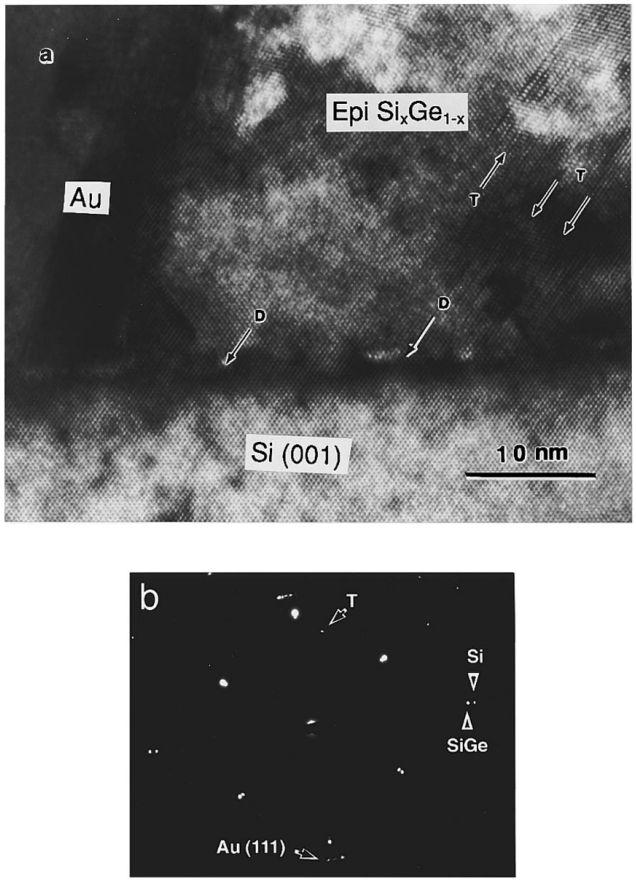


FIG. 6. (a) High-resolution image of a specimen annealed to 150 °C, taken at the [011] zone axis. The continuity of the {111} lattice fringes across the Si_xGe_{1-x}/sc-Si interface demonstrates the epitaxial relationship between Si_xGe_{1-x} and Si(001). Twins (T) in the epitaxial island, and misfit dislocations (D) at the interface are indicated by arrows. (b) Diffraction pattern showing the epitaxial relationship between Si_xGe_{1-x} and Si(001). The objective aperture included the Si_xGe_{1-x} twin reflection "T" and excluded Au(111) reflections during phase contrast imaging.

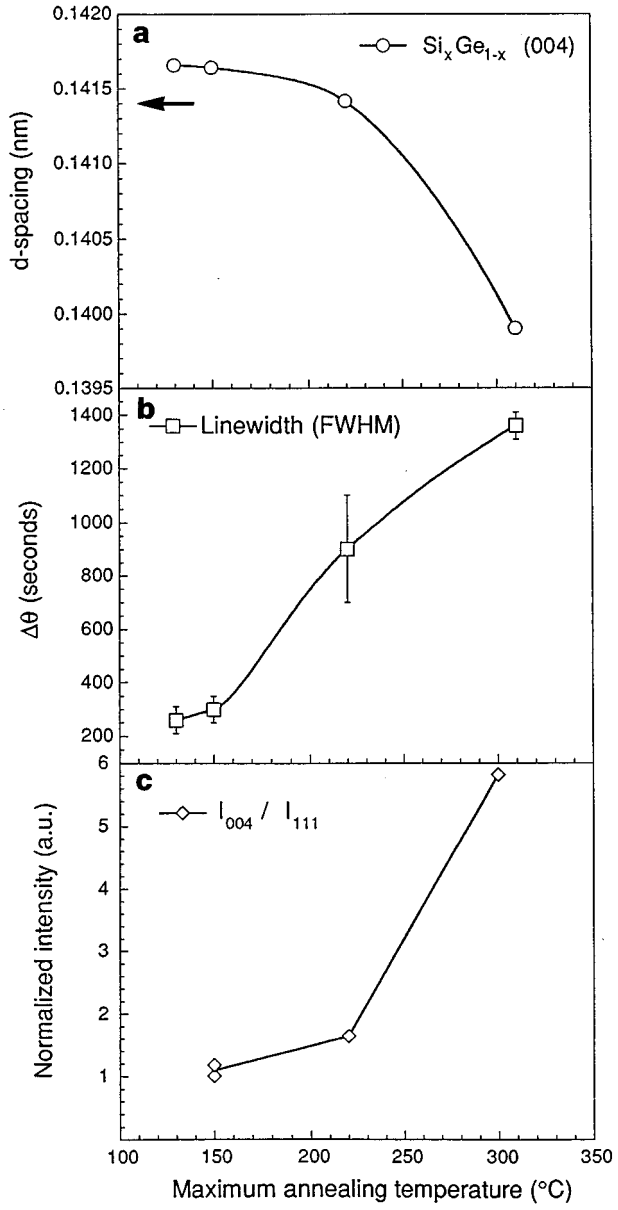


FIG. 7. XRD results showing the variation of (a) (004) d spacing of the Si_xGe_{1-x} (arrow indicates the d spacing for pure Ge: 0.1414 nm); (b) linewidth; and (c) the relative intensity of Si_xGe_{1-x} (004) XRD peak, plotted as a function of the maximum annealing temperature. (a) and (b) were determined from rocking curve ω scans, while (c) was determined by θ–2θ scans after misaligning the sample by 2° with respect to the sc-Si substrate. Bold curves are drawn through the data points to depict the trend in the variation of the respective parameters in the different graphs.

epitaxially on sc-Si at locations separated by the Au grains. The lattice image of one such island of epitaxial Si_xGe_{1-x} on sc-Si is shown in Fig. 6(a). The lattice spacing of Au could not be resolved due to instrument limitation. Misfit dislocations were observed at the Si_xGe_{1-x}/sc-Si interface (originally the Au/sc-Si interface) indicating that the epilayer was at least partly relaxed at 150 °C. Planar defects observed in the Si_xGe_{1-x} epilayer were identified to be (111) twins from the analysis of diffraction patterns. A representative diffraction pattern is shown in Fig. 6(b).

XRD spectra of crystallized Si_xGe_{1-x} were analyzed for samples annealed to different temperatures. The results of this XRD analysis are summarized in Fig. 7. The increase in the relative intensity of the (004) Si_xGe_{1-x} XRD peak [normalized to the (111) Si_xGe_{1-x} intensity] qualitatively shows the increasing preference of (004) planes of the crystallized Si_xGe_{1-x} grains to be oriented parallel to the surface of the film with increasing temperature. The d spacing of the (004) planes of the crystallized layer decreased, while the linewidth of the (004) epilayer peak increased with increasing temperature.

Samples annealed to 310 °C had a laterally continuous epitaxial Si_xGe_{1-x} film on the sc-Si substrate. This is elucidated by the bright-field TEM micrograph in Fig. 8(a) and the diffraction pattern in Fig. 8(b). It is interesting to note that the thickness of the epilayer was the same as the initial thickness of the as-deposited Au film, and that the initial a-Ge/Au interface was preserved. Analysis of diffraction patterns taken at different zone axes revealed the occurrence of sets of Bragg reflections in pairs. The patterns were similar to those shown in Fig. 6(b) and were identified to be a juxtaposition of two sets of diffraction spots, namely: one aris-

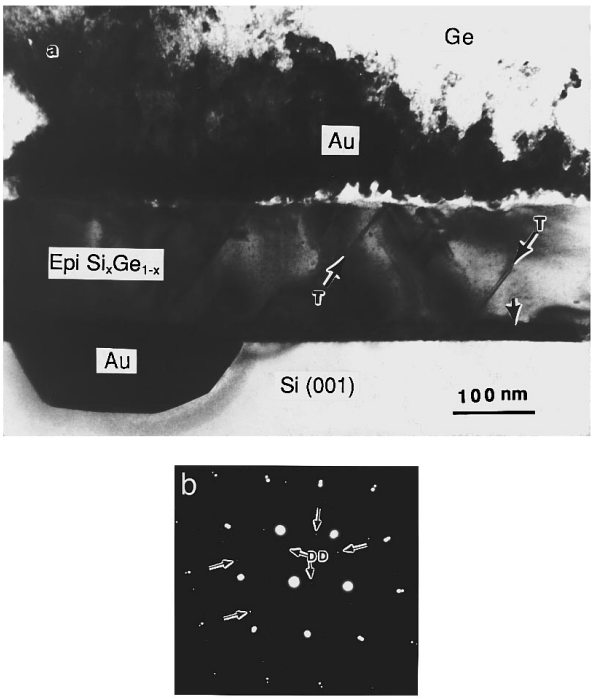


FIG. 8. (a) Bright-field TEM micrograph showing the configuration of a sample annealed to 310 °C. Arrows indicate twinning in the epilayer (marked *T*), and remnant Au in the epilayer near the Si_xGe_{1-x}/sc-Si interface (unlabeled). (b) A [011] zone axis diffraction pattern showing the occurrence of spots of Si_xGe_{1-x} and sc-Si in pairs (inner spots ⇔ Si_xGe_{1-x} alloy, outer spots ⇔ sc-Si). The orientation of the spot pairs illustrates the epitaxial relationship between Si_xGe_{1-x} and sc-Si. Representative extra spots arising due to twinning (unlabeled) across the {111} planes in the Si_xGe_{1-x} film, and double diffraction (marked "DD") are indicated by arrows.

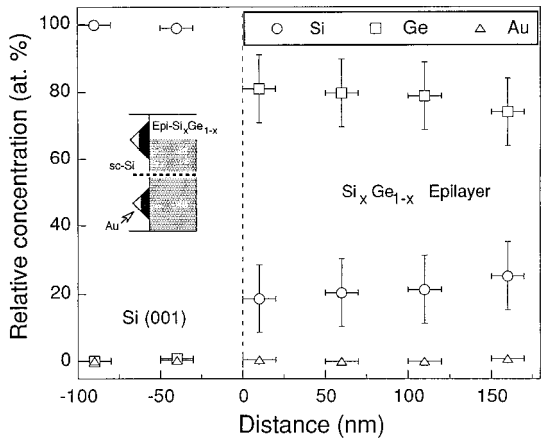


FIG. 9. A representative XEDS line scan profile (dashed line in the schematic drawing) across the thickness of the Si_xGe_{1-x} epilayer in a sample annealed to 310 °C. Note that there are no drastic variations in the Si content (≈20 at. %) across the epilayer.

ing from the sc-Si substrate, and another from the Si_xGe_{1-x} epilayer. The outer set of spots (lower *d* spacing) were identified to correspond to the sc-Si substrate and the inner set of spots correspond to the Si_xGe_{1-x} epilayer which has a higher lattice spacing. The relative orientation of the two sets of spots in reciprocal space unambiguously demonstrates the epitaxial relationship of the Si_xGe_{1-x} layer with the sc-Si substrate. Diffraction patterns also showed extra reflections due to twins in the epilayer, and double diffraction. Twins running across the entire thickness of the epilayer was a common occurrence, as was the presence of residual quantities of Au near the epitaxial Si_xGe_{1-x}/sc-Si interface (Au/Si interface in the as-deposited sample). However, no threading dislocations were observed. Pyramid-shaped spikes filled with Au [see Fig. 8(a)] were observed in the substrate because of the preferential dissolution of Si into the Au film from the (111) planes of sc-Si at localized places in the substrate during the incorporation of Si in the epilayer. Often, nontriangular sections of the pyramid were observed during TEM [as in Fig. 8(a)] because slicing through the apex of a pyramid to yield a triangular section during TEM sample preparation is a relatively rare occurrence.

XEDS analysis (see Fig. 9) showed that the nominal concentration of Si in the epilayer was approximately ≈20 at. % and was uniform both laterally and vertically across its thickness. The Au concentration was below the XEDS detection limit across the entire thickness of the epilayer except for the region near the Si_xGe_{1-x}/sc-Si interface. RBS measurements on samples with the top layer etched off showed that the Si content in the Si_xGe_{1-x} epilayer was $x \approx 15$ at. % (see Fig. 10), which is in good agreement with the XEDS measurements. TEM and XEDS showed that above 300 °C, the top layer consisted of discontinuously dispersed Au grains in a matrix of completely crystallized Ge. The discontinuity of the Au grains in the top layer is the likely reason for the large increase in resistance at ≈270 °C.

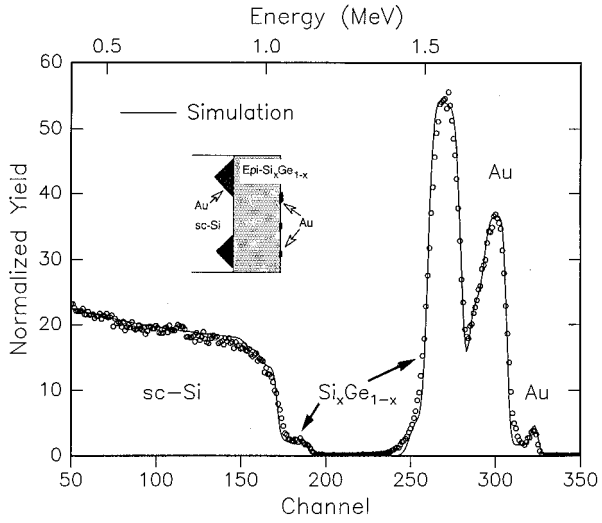


FIG. 10. Experimentally determined (circles) and simulated (bold curve) RBS spectra for a sample annealed to 310 °C. The surface Au peak is due to the presence of residual Au (not removed completely during etching) on the surface of the epilayer. The large Au peak is due to the remnant Au lodged in the pyramid shaped spikes in the sc-Si and at the epi-Si_xGe_{1-x} interface (see drawing). Arrows indicate the RBS peaks of Si and Ge arising from the epilayer. The Si content in the epilayer was found to be ≈15 at. %.

IV. DISCUSSION

The sequence of changes leading to the SPE growth of a Si_xGe_{1-x} alloy layer on sc-Si during thermal annealing of *a*-Ge/Au bilayers was studied. Sheet resistance results showed that below 70 °C there were no appreciable changes in the microstructure of the thin film sandwich. However, the sheet resistance being insensitive to the morphology of the *a*-Ge layer in this temperature range, it is possible that the collapse (observed at 150 °C) of the columnar void structure may have already begun below 70 °C. The decrease in the sheet resistance observed in Au/sc-Si, Au/SiO_2, and *a*-Ge/Au/sc-Si was due to the grain growth that occurred in the Au film between ~80 and 120 °C. The increase in the grain size resulted in reduced grain boundary scattering, causing a decrease in the sheet resistance. This is consistent with our earlier work[11] and surface energy driven grain growth in Au films known to occur at low temperatures.[21]

At temperatures above ≈130 °C, various processes leading to the reversal of the *a*-Ge and the Au layers, and the crystallization of Ge were observed. The diffusion and incorporation of Ge between Au grains and the release of Au to the top layer caused the fragmentation of the Au film and reduced the number of low resistance paths provided by the initially continuous Au film. This increased the effective resistance of the Au film, due to the high resistivity of Ge compared to that of Au,[19] and is largely responsible for the sharp rise in sheet resistance at ≈130 °C. The variation in the actual value of the increase in resistance is due to local variations in the Au film microstructure (e.g., thickness, grain size, etc.), as these parameters would determine the extent of Ge incorporation and hence the extent of fragmentation of the Au film.

The Au appeared to have diffused through the columnar voids in the *a*-Ge film, over distances which are three orders of magnitude larger than that calculated from the reported value of the diffusion coefficient of Au in bulk Ge.[22] This is most likely due to the short-cut diffusion path provided by the columnar void structure in the *a*-Ge layer. Furthermore, the Au that diffuses into the Ge layer satisfies the Ge dangling bonds in the void structure and the resulting reduction in free energy enhances the driving force for diffusion. Our observation of the formation of clusters of Au in the *a*-Ge layer is supported by the recent work of Edwards and co-workers[23] who have reported the formation of clusters of Au and intermetallic-type Au–Ge compound(s) in an *a*-Ge matrix. The intermixing that occurs at the *a*-Ge/Au interface during annealing is conducive for the clustering of Au or possibly the formation of a metastable Au–Ge alloy on the *a*-Ge side of the interface. The insensitivity of the sheet resistance between 150 and 270 °C may be due to a low resistance path provided by a network of Au crystallites, on the Ge side of the initial *a*-Ge/Au interface [see Fig. 4(a)] that effectively offsets the increase in resistance due to incorporation of Ge in the grain boundaries of the Au film. The crystallization of Ge at temperatures near 130 °C (which is far below the crystallization temperature of Ge) is a consequence of metal-induced crystallization typical in low-temperature eutectic systems.[24] The crystallization temperature is reduced because of the enhanced mobility of Ge due to its interaction with Au. The observed temperature of Au-mediated crystallization, is close to ≈0.6 T_E(Au–Ge eutectic temperature—361 °C)[20] in good agreement with earlier predictions.[24] The mechanism of Au-mediated crystallization may be related to the modification of the local structure of *a*-Ge[23] brought about by the presence of Au.

The Ge that diffused through the Au grain boundaries, incorporated some Si and grew epitaxially on sc-Si between Au grains. These epitaxial islands of Si_xGe_{1-x} were isolated from each other by the intervening Au grains. The fact that Ge diffused primarily through the grain boundaries of Au indicates that the microstructure of the initial Au layer is an important parameter that affects the SPE process. The (111)-type planar defects observed by TEM are indicative of a three-dimensional growth mechanism. The XEDS results, which indicate high Si content in Au strongly suggest that the Si dissolved in the Au grains before entering the growing epitaxial islands between the Au grains. This inference is in agreement with the work of Hiraki and co-workers[25] who have shown that appreciable amounts of Si can diffuse through Au grains at very low temperatures. It has been shown that Si that dissolved into the Au grains segregated and accumulated at the surface.

In the present situation, the Si is likely to have segregated to the surface as well as grain boundaries, thus feeding Si to the epitaxial islands growing between Au grains. The accumulation of Si on the surface of the Au grains during or after TEM sample preparation may also be the reason for the Si content to show up as being much higher than the equilibrium solubility limit of Si in Au. The dissolution of Si in Au is the likely reason for the lateral and vertical uniformity in the composition of the final epilayer. If Si had entered the epilayer directly from the substrate, lateral, and vertical nonuniformity in composition would have been expected, which is contrary to our observations. In an earlier article[26] it was assumed that the epilayer at 150 °C was pure Ge, owing to the uncertainty of the Si content as determined by XEDS. In this work, the Si content determined by XEDS is assumed to be a qualitative indication of the actual composition, as the XEDS measurements have been shown to be in good agreement with the RBS results for the composition of the epilayer at 310 °C.

The (004) *d* spacing of a Si_xGe_{1-x} ($x \approx 0.15$) epilayer with no residual stresses should be less than that of pure Ge. However, XRD results showed that between 130 and 150 °C the (004) *d* spacing of the Si_xGe_{1-x} film (perpendicular to the plane of the film) was greater than that of pure Ge. This is an indication of the film being pseudomorphic with respect to the substrate. The larger *d* spacing is a manifestation of the Poisson relaxation perpendicular to the plane of the film, caused by compressive residual stresses in the plane of the film. Estimation of the relaxation parameter from the equations used by Zaumseil,[27] assuming the Si_xGe_{1-x} epilayer to contain ≈15 at. % Si, showed that the epilayer was ≈70% strain-relaxed at 150 °C. The decrease in the (004) *d* spacing of the Si_xGe_{1-x} epilayer with increasing temperature is attributed to relaxation of residual strain and increasing Si content. On annealing to 310 °C, the Si_xGe_{1-x} epilayer was determined to be completely relaxed. This strain relaxation

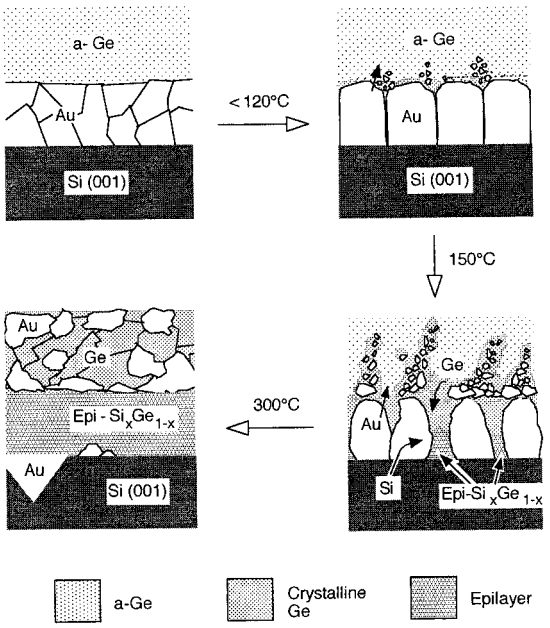


FIG. 11. A schematic illustration of the sequence of processes occurring during annealing of *a*-Ge/Au/sc-Si sandwiches from room temperature to 300 °C at 1 °C/min. The white regions represent Au grains.

during the epitaxial growth of Si_xGe_{1-x} alloy may be the reason for the absence of threading dislocations.[28]

The enhancement of the (004) texture of the Si_xGe_{1-x} alloy qualitatively indicated the increasing volume fraction of epitaxial Si_xGe_{1-x} on sc-Si with increasing temperature. The displacement of the Au layer to the top facilitated the lateral growth of the epitaxial islands. These epitaxial islands coalesced when the Au between them was displaced completely, to form a laterally continuous layer of Si_xGe_{1-x} on Sc-Si. The final thickness of the Si_xGe_{1-x} epilayer at 310 °C being the same as that of the initial Au layer suggests the active participation of Au throughout the epitaxial growth process. Thus, it is inferred that the thickness of the Au layer limits the thickness of the heteroepitaxial layer in Au-mediated SPE. The increasing linewidth of the (004) epilayer peak is attributed to the deterioration of the quality of the epitaxial layer caused by formation of defects[29] such as twins and stacking faults (observed by TEM) to accommodate the misfit between the epitaxial islands during their coalescence.

In summary, Au-mediated SPE growth of a Si_xGe_{1-x} alloy on Si(001) was initiated between Au grains below $\approx$130 °C. The grain boundaries of Au provide a fast diffusion path for the diffusion and crystallization of Ge, as Si entered the epilayer after dissolving in the Au grains. The void structure in the *a*-Ge film was a short-cut diffusion path for Au, which is responsible for locally crystallizing Ge below 130 °C. The displacement of Au enabled the layer reversal of Au and Ge and facilitated the lateral growth and coalescence of the epitaxial islands yielding a laterally continuous Si_xGe_{1-x} epilayer of uniform composition. The top layer finally comprised discontinuously dispersed grains of Au and Ge. A schematic sketch of the sequence of processes occurring during annealing is summarized in Fig. 11. The driving forces involved in the SPE process are the reduction in the free energy due to the crystallization of Ge and the reduction in the interfacial energy due to the epitaxial relationship of Si_xGe_{1-x} islands with the substrate. The latter is also the driving force for the coalescence of the epitaxial islands that were initially isolated.

V. CONCLUSIONS

Au-mediated SPE heteroepitaxial growth of Si_xGe_{1-x} alloys on Si(001) is a complicated process. Au-mediated Ge crystallization at the *a*-Ge/Au interface, and the onset of growth of epitaxial Si_xGe_{1-x} on sc-Si occurred at temperatures below 130 °C. The microstructure of the Au layer is a critical parameter in the SPE process. Ge diffused predominantly through the grain boundaries of Au and initiated the epitaxial growth of Si_xGe_{1-x} islands on the Si substrate. The Si from the substrate dissolved in the Au grains before entering the epilayer. On annealing to 310 °C a laterally continuous, strain-relaxed Si_xGe_{1-x} epilayer of uniform composition ($x \approx 0.15$) was obtained. The final thickness of the epilayer appeared to be limited by the initial thickness of the Au layer. The principal defects observed in the epilayer were twins, and residual Au trapped at the epi-Si_xGe_{1-x}/sc-Si interface.

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